A6610

Datasheet (Brief)

AIXLINK

Version 1.0
Copyright© 2023.03
寰宇智芯

Revision History

Date	Version	Summary of Changes
2023.03	1.0	First Release

Note:

Adding/ Removing contents in this document may create a numbering mismatching of sections, tables, pictures existing in the revision history above over the time. And the associated cross-references could be useless because the pointed objects are different than expected or don't exist anymore.

Revision History

Notice

1. Disclaimer

AIXLINK® releases no license, whether express, implied, arising by estoppel or otherwise, of any intellectual property right is granted by this document.

AIXLINK® makes no representations or warranties with respect to the accuracy or completeness of the contents of this document.

AIXLINK® reserves the right to discontinue or make changes to specifications and product descriptions at any time without notice.

AIXLINK® assumes no liability for any damages or consequences resulting from the use of this document.

AIXLINK® strongly recommended to contact the local sales office to obtain the latest specifications and product descriptions as well as any other useful detail before placing any order.

2. Copyright and confidentiality

3. Acknowledgement

Third-party brands and names mentioned in this document are for identification purpose only and may be the property of their respective owners.

Supply of this implementation of Third-party Technology does not convey a license nor imply a right under any patent, or any other industrial and intellectual property right of Third-party to use this implementation in any finished end-user and ready-to-use final product.

Besides it is hereby notified that a license for such use is required from Third-party.

About

1. Mission of the document

This document provides general information about A6610 SoC. In addition to providing board diagrams, this document also addresses pin characteristics and signal description.

2. Target audience

By reason of high level of the covered topics, the reading of this document is mainly intended to aid:

- ➢ FAE engineers
- ➢ Hardware design engineers

This document contains confidential proprietary information that is solely for authorized personnel. It is not to be disclosed to any unauthorized person without prior written consent of AIXLINK® Corporation.

3. Main references

It's recommended to keep contact with AIXLINK® R&D Dept. to get the newest updates.

Contents

List of Figures

List of Tables

1. Overview

A6610 SOC chip is a highly integrated SOC for IOT solution with 2.4GHz Wi-Fi and BLE. It (A6610) also includes Andes MCU, Crypto engine, SDIO2.0, SPI, ... and various peripheral interfaces to have high reliability and low power consumption to fulfill various consumer applications. A6610 can be used for Low-Power IOT platform solutions.
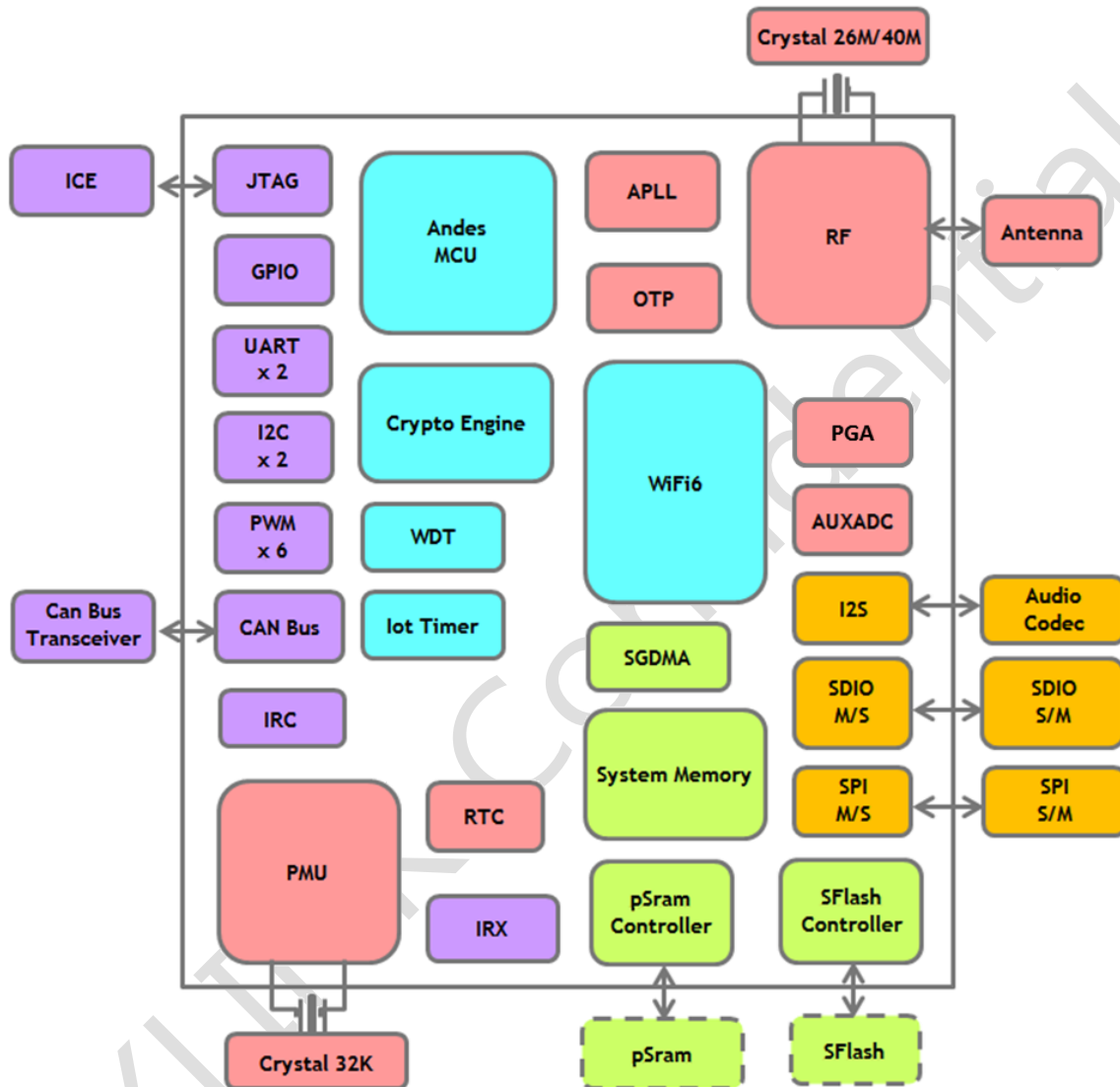

Figure 1: Architecture Block Diagram

1.1 Wi-Fi Key Features

➢ Compliant to 802.11a/b/g/n/ax up to 114.7Mbps phy-rate @2.4GHz
➢ OFDMA & MU-MIMO as a STA
➢ QoS, A-MPDU & hardware de-fragmentation
➢ Handle the Wi-Fi & BLE Co-existence

1.2 Bluetooth LE Key Features

➢ Bluetooth LE Class 1.5 or Class 2 transmitter operation
➢ Bluetooth LE 5.1 Ready
➢ Support all BLE5.0 optional features including LE-2Mbps, LE-Long Range, LE-Advertising Extensions
➢ Dedicated BLE path for best Coex performance
➢ Interface support, host controller

interface (HCI) using a high speed UART interface

➢ AT Commands support

1.3 MCU and Advanced Features

1.3.1 CPU and Memory

➢ Andes N25F MCU core, compliant to RV32IMAFN of RISC-V ISA extensions, provides up to 520 DMIPS@184 MHz
➢ 212 KB ROM
➢ 664 KB SRAM
➢ 8 KB SRAM in RTC
➢ Embedded 4MB flash and 8MB pseudo-SRAM

1.3.2 Clocks and Timers

➢ External 26 MHz/40 MHz crystal oscillator
➢ An optional external 32 KHz crystal oscillator
➢ One 64-bit timer and 5 × 32-bit timers
➢ One 44-bit RTC timer

1.3.3 Advanced interface port

➢ 20 independent GPIO port
➢ 12-bit SAR ADC with up to 4 channels of ACC and increased 16-bit resolution

➢ 1 SPI Master/Slave
➢ 1 I²S Master
➢ 2 I²C Master
➢ 2 UART
➢ 6 PWM
➢ 1 IR TX/RX
➢ 1 Host/Slave SDIO
➢ CAN 2.0

1.3.4 Security

➢ Secure boot
➢ Flash decryption
➢ 8192-bit OTP, up to 2048-bit for customers
➢ Cryptographic hardware engine:
  • Multiple HW-based cryptographic standards acceleration
  • Key management
  • DMA
  • True Random Number Generator (TRNG)

1.4 Applications (examples)

➢ Generic IoT Sensor Hub
➢ Generic IoT Data Loggers
➢ IoT Mesh Network
➢ Home Automation
  • Smart Light control
  • Smart plugs
  • Energy monitoring
➢ Industrial Automation
  • Industrial wireless control
  • Industrial CAN gateway
➢ Audio Applications
  • Internet music players

➢ Video Applications
  • Cameras
  • Image Recognition
  • Over-the-top Devices
➢ Toys Applications
  • Remote control toys
  • Educational robots toys
  • Voice toys
➢ Retail Applications
  • POS machines
  • PDA machines
  • Service robots

- Audio streaming devices
- Audio headsets

➢ Health Applications

2. Pin Definitions

2.1 Pin Layout

Figure 2: Pin Layout (QFN 5*5 Top view)

3. Ordering Information

Table 1: Ordering Information

Ordering code	Package	Embedded Information
A6610A-Q540	QFN 5x5	4MB Flash
A6610A-Q548	QFN 5x5	4MB Flash + 8MB PSRAM