A6610

Datasheet (Brief)

Version 1.2

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Revision History

Date	Version	Summary of Changes
2023.03	1.0	First Release
2023.03	1.1	Add PDA machines to 1.4 Retail applications Add PGA to Figure 1
2023.05	1.2	Updated 1.Overview Figure 1: Architecture Block Diagram 1.3.4 Security

Note:

Adding/ Removing contents in this document may create a numbering mismatching of sections, tables, pictures existing in the revision history above over the time. And the associated cross-references could be useless because the pointed objects are different than expected or don't exist anymore.

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About

1. Mission of the document

This document provides general information about A6610 SoC. In addition to providing board diagrams, this document also addresses pin characteristics and signal description.

2. Target audience

By reason of high level of the covered topics, the reading of this document is mainly intended to aid:

- FAE engineers
- Hardware design engineers

3. Main references

It's recommended to keep contact with AIXLINK® R&D Dept. to get the newest updates.

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1. Overview

A6610 SOC chip is a highly integrated SOC for IOT solution with 2.4GHz Wi-Fi and BLE. It (A6610) also includes Andes MCU, SDIO2.0, SPI, ... and various peripheral interfaces to have high reliability and low power consumption to fulfill various consumer applications. A6610 can be used for Low-Power IOT platform solutions.

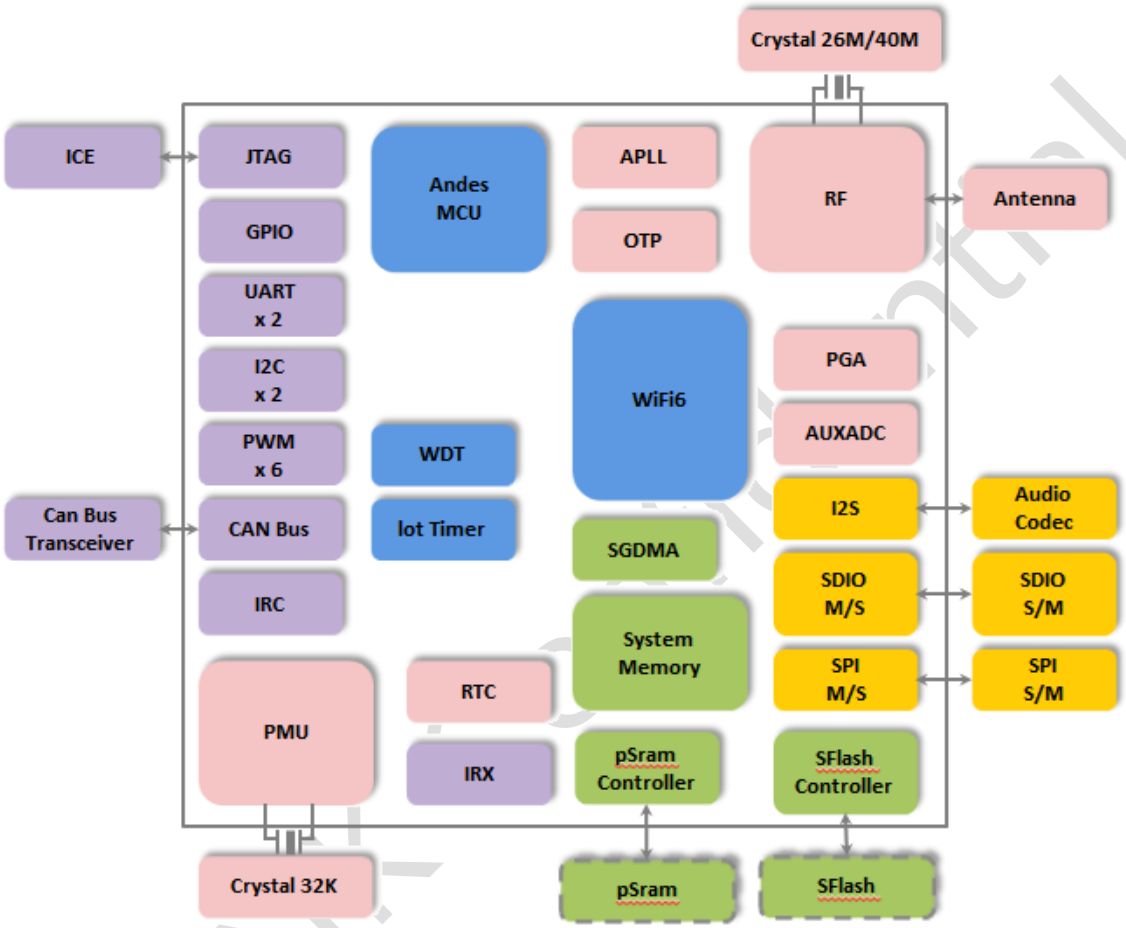

Figure 2: Architecture Block Diagram

1.1 Wi-Fi Key Features

- Compliant to 802.11a/b/g/n/ax up to 114.7Mbps phy-rate @2.4GHz
- OFDMA & MU-MIMO as a STA
- QoS, A-MPDU & hardware de-fragmentation
- Handle the Wi-Fi & BLE Co-existence

1.2 Bluetooth LE Key Features

- Bluetooth LE Class 1.5 or Class 2 transmitter operation
- Bluetooth LE 5.1 Ready
- Support all BLE5.0 optional features including LE-2Mbps, LE-Long Range, LE-Advertising Extensions
- Dedicated BLE path for best Coex performance
- Interface support, host controller interface (HCI) using a high speed UART interface
- AT Commands support

1.3 MCU and Advanced Features

1.3.1 CPU and Memory

- Andes N25F MCU core, compliant to RV32IMAFN of RISC-V ISA extensions, provides up to 520 DMIPS@184 MHz
- 212 KB ROM
- 664 KB SRAM
- 8 KB SRAM in RTC
- Embedded 4MB flash and 8MB pseudo-SRAM

1.3.2 Clocks and Timers

- External 26 MHz/40 MHz crystal oscillator
- An optional external 32 KHz crystal oscillator
- One 64-bit timer and 5 × 32-bit timers
- One 44-bit RTC timer

1.3.3 Advanced interface port

- 20 independent GPIO port
- 12-bit SAR ADC with up to 4 channels of ACC and increased 16-bit resolution
- 1 SPI Master/Slave
- 1 I²S Master
- 2 I²C Master
- 2 UART
- 6 PWM
- 1 IR TX/RX
- 1 Host/Slave SDIO
- 1 CAN 2.0

1.3.4 Security

- Flash decryption
- 8192-bit OTP, up to 2048-bit for customers

1.4 Applications (examples)

- Generic IoT Sensor Hub
- Generic IoT Data Loggers
- IoT Mesh Network
- Home Automation
  - Smart Light control
  - Smart plugs
  - Energy monitoring
- Industrial Automation
  - Industrial wireless control
  - Industrial CAN gateway
- Audio Applications
  - Internet music players
  - Audio streaming devices
  - Audio headsets
- Video Applications
  - Cameras
  - Image Recognition
  - Over-the-top Devices
- Toys Applications
  - Remote control toys
  - Educational robots toys
  - Voice toys
- Retail Applications
  - POS machines
  - PDA machines
  - Service robots
- Health Applications

2. Pin Definitions

2.1 Pin Layout

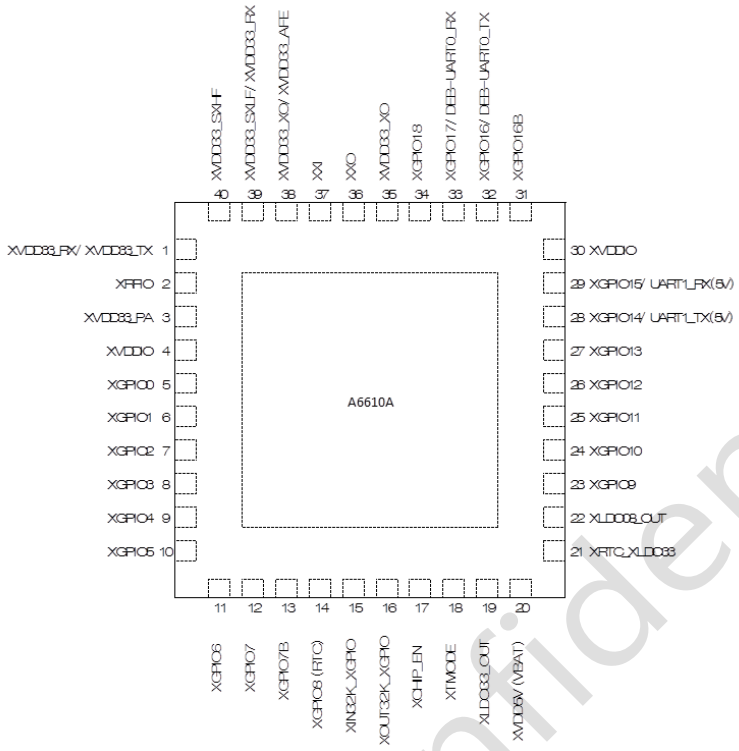

Figure 3: Pin Layout (QFN 5*5 Top view)

3. Ordering Information

Table 1: Ordering Information

Ordering code	Package	Embedded Information
A6610A-Q540	QFN 5x5	4MB Flash
A6610A-Q548	QFN 5x5	4MB Flash + 8MB PSRAM